WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a plurality of memory cells each drawing cell current according to data stored therein when selected;

a plurality of word lines and a plurality of bit lines selected for accessing data in a specific memory cell among the plurality of memory cells;

a power supply for providing a voltage corresponding to a high-level side potential of data in the plurality of memory cells;

a word line potential supply source for supplying a potential to the plurality of word lines; and

a precharge potential supply source for supplying a precharge potential to the plurality of bit lines,

wherein a precharge potential supplied to non-selected bit lines among the plurality of bit lines by the precharge potential supply source is set at a value lower than the voltage of the power supply,

a potential supplied to non-selected word lines among the plurality of word lines by the word line potential supply source is set at a predetermined negative value, and

a total of the absolute value of the precharge potential of the non-selected bit lines supplied by the precharge potential supply source and the absolute value of the potential of the non-selected word lines supplied by the word line potential supply source is a value less than the voltage of the power supply.

2. The device of Claim 1, wherein the precharge potential of the non-selected bit lines supplied by the precharge potential supply source is set at a value less than half of the voltage of the power supply.

3. The device of Claim 1, wherein a precharge potential supplied to a selected bit line among the plurality of bit lines by the precharge potential supply source is set at a value higher than the precharge potential supplied to the non-selected bit lines by the precharge potential supply source and equal to or more than the half of the voltage of the power supply.

4. The device of Claim 1, wherein each of transistors constituting the plurality of memory cells is constructed of a transistor in which the difference in current amount per unit gate width between OFF leakage current and gate leakage current is within two orders of magnitude.

5. The device of Claim 1, wherein the voltage of the power supply is 0.5 V to 1.2 V.

6. The device of Claim 1, wherein the negative potential supplied to the non-selected word lines by the word line potential supply source is changed depending on ambient temperature.

7. The device of Claim 6, wherein the absolute value of the negative potential supplied to the non-selected word lines by the word line potential supply source is larger when the ambient temperature is high than when it is normal.

8. A semiconductor memory device comprising:

a plurality of memory cells each drawing cell current according to data stored therein when selected;

a plurality of word lines and a plurality of bit lines selected for accessing data in a specific memory cell among the plurality of memory cells;

a power supply for providing a voltage corresponding to a high-level side potential of data in the plurality of memory cells;

a plurality of source lines for supplying a low-level side potential of data in the plurality of memory cells;

a word line potential supply source for supplying a potential to the plurality of word lines;

a precharge potential supply source for supplying a precharge potential to the plurality of bit lines; and

a source potential supply source for supplying a potential to the plurality of source lines,

wherein a precharge potential supplied to non-selected bit lines among the plurality of bit lines by the precharge potential supply source is set at a value lower than the voltage of the power supply,

a potential supplied to non-selected word lines among the plurality of word lines by the word line potential supply source is set at a predetermined negative value,

a potential supplied to non-selected source lines among the plurality of source lines by the source potential supply source is set at a predetermined positive value,

a total of the absolute value of the precharge potential of the non-selected bit lines supplied by the precharge potential supply source and the absolute value of the potential of the non-selected word lines supplied by the word line potential supply source is set at a value less than the voltage of the power supply, and

the absolute value of the potential of the non-selected word lines supplied by the word line potential supply source and the absolute value of the potential of the non-

selected source lines supplied by the source potential supply source are roughly equal to each other.

9. The device of Claim 8, further comprising a row decode circuit for selecting a word line from the plurality of word lines according to a row address received,

wherein selection and non-selection of the plurality of source lines is performed based on the row address.

10. The device of Claim 8, further comprising a column decoder for selecting a bit line pair from the plurality of bit lines according to a column address received,

wherein selection and non-selection of the plurality of source lines is performed based on the column address.

11. The device of Claim 8, wherein the positive potential supplied to the non-selected source lines by the source line potential supply source is changed depending on ambient temperature.

12. The device of Claim 11, wherein the positive potential supplied to the non-selected source lines by the source line potential supply source is larger when the ambient temperature is high than when it is normal.

13. The device of Claim 6, wherein the semiconductor memory device is used for portable equipment having a normal operation mode and a standby mode, and

the potential is changed depending on the ambient temperature for the normal operation mode and the standby mode separately.

14. The device of Claim 11, wherein the semiconductor memory device is used for portable equipment having a normal operation mode and a standby mode, and

the potential is changed depending on the ambient temperature for the normal operation mode and the standby mode separately.

15. A semiconductor integrated circuit comprising:

a semiconductor memory including a plurality of memory cells, a plurality of word lines and a plurality of bit lines selected for accessing data in a specific memory cell among the plurality of memory cells, a decode circuit for selecting any word line from the plurality of word lines, and a word line drive circuit for driving the selected word line in response to an output of the decode circuit received; and

a semiconductor circuit including a transistor having a low threshold voltage and a transistor having a high threshold voltage,

wherein the decode circuit of the semiconductor memory has a transistor of which a source line is connected to the ground potential, the transistor being constructed of a transistor having a low threshold voltage of the same type as the transistor having a low threshold voltage included in the semiconductor circuit, and

the word line drive circuit of the semiconductor memory has a pull-down transistor of which a source line for pulling down the potential of the word line is connected to a negative potential supply line, the pull-down transistor being constructed of a transistor having a high threshold voltage of the same type as the transistor having a high threshold voltage included in the semiconductor circuit.

16. The circuit of Claim 15, wherein the absolute value of the high threshold

voltage of the pull-down transistor of the word line drive circuit is equal to or larger than the absolute value of the potential of the negative potential supply line.

17. The circuit of Claim 15, wherein the pull-down transistor of the word line drive circuit includes a parallel circuit having:

a transistor having a low threshold voltage of which a source line is connected to the ground line; and

a transistor having a high threshold voltage of which a source line is connected to the negative potential supply line.

18. The circuit of Claim 15, wherein in the semiconductor circuit, the transistor having a low threshold voltage is a transistor including a gate oxide film or threshold adjusting impurity formed for a transistor constituting a logic circuit that is high in leakage current but operates at high speed, and

the transistor having a high threshold voltage is a transistor including a gate oxide film or threshold adjusting impurity formed for a transistor constituting a logic circuit that operates at low speed but is low in leakage current.

19. The circuit of Claim 15, wherein in the semiconductor circuit, the transistor having a low threshold voltage is a transistor including a gate oxide film or threshold adjusting impurity formed for a transistor constituting a logic circuit, and

the transistor having a high threshold voltage is a transistor including a gate oxide film or threshold adjusting impurity formed for a transistor constituting an analog circuit and/or an I/O circuit.

20. The circuit of Claim 15, wherein the power supply voltage supplied to the semiconductor memory and the semiconductor circuit is 0.5 V to 1.2 V.

21. The device of Claim 1, wherein the semiconductor memory device is an SRAM.

22. The device of Claims 8, wherein the semiconductor memory device is an SRAM.

23. The device of Claims 1, wherein the semiconductor memory device is a ROM.

24. A semiconductor integrated circuit comprising:

the semiconductor memory device of Claim 1; and

a semiconductor circuit including a transistor having a low threshold voltage and a transistor having a high threshold voltage,

wherein the absolute value of the negative potential supplied to the non-selected word lines by the word line potential supply source of the semiconductor memory device is equal to or smaller than the absolute value of the high threshold voltage of the transistor of the semiconductor circuit.